



AF/IFw

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Mail Stop Appeal Brief –Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

October 25, 2007

  
Sherri A. Phillips

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Appl. No. : 10/773,583

Confirmation No. : 6732

Applicants : Douglas A. Larson and Jeffrey J. Cronin

Filed : February 5, 2004

Attorney Docket No.: 501296.01 (30266/US)

Art Unit : 2188

Customer No. : 27,076

Examiner : Duc T. Doan

Title : APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL  
DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM

---

**AMENDED APPEAL BRIEF TRANSMITTAL**

Mail Stop Appeal Brief –Patents  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Transmitted herewith, in triplicate, is the Amended Appeal Brief in this application, with respect to the Notice of Appeal filed on April 5, 2007 and the Appeal Brief filed June 5, 2007. Fees associated with filing of the Appeal Brief were previously paid.

Any deficiency or overpayment should be charged or credited to Deposit Account No. 50-1266. This transmittal is being submitted in duplicate.

Respectfully submitted,

DORSEY & WHITNEY LLP



Karen Lenaburg  
Registration No. 58,371

KL:sp

Enclosures:

Postcard

Amended Appeal Brief (+ 2 copies)

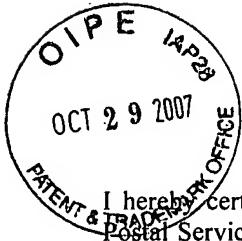
Copy of this Transmittal

1420 Fifth Avenue, Suite 3400

Seattle, WA 98101

Tel: (206) 903-8800

Fax: (206) 903-8820



PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450. Alexandria, VA 22313-1450.

Date

October 25, 2007

  
Sherri A. Phillips

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Appl. No. : 10/773,583	Confirmation No. : 6732
Applicants : Douglas A. Larson and Jeffrey J. Cronin	
Filed : February 5, 2004	Attorney Docket No.: 501296.01 (30266/US)
Art Unit : 2188	Customer No. : 27,076
Examiner : Duc T. Doan	
Title : APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM	

---

Mail Stop Appeal Brief – Patents  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**APPELLANTS' AMENDED BRIEF (37 C.F.R. § 41.37)**

Sir:

This brief is in furtherance of the Notice of Appeal filed in this case on April 5, 2007 and the Appeal Brief filed on June 5, 2007. The fees required under Section 41.20, and any required request for extension of time for filing this brief and fees therefore, are dealt with in the accompanying transmittal letter.

## TABLE OF CONTENTS

<u>Section</u>	<u>Page Number</u>
I. REAL PARTY IN INTEREST.....	3
II. RELATED APPEALS AND INTERFERENCES .....	4
III. STATUS OF CLAIMS.....	5
IV. STATUS OF AMENDMENTS.....	6
V. SUMMARY OF CLAIMED SUBJECT MATTER.....	7
VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL .....	9
VII. ARGUMENTS .....	10
VIII. CLAIMS APPENDIX .....	16
IX. EVIDENCE APPENDIX .....	18
X. RELATED PROCEEDINGS APPENDIX.....	19
XI. CONCLUSION .....	20

## I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee of this application, Micron Technology, Inc., a Delaware Corporation having a principal place of business in Boise, Idaho.

## II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to appellants, the Appellants' legal representative, or the assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

### III. STATUS OF CLAIMS

#### A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-43.

#### B. STATUS OF ALL THE CLAIMS

1. Claims canceled: 1-39.
2. Claims withdrawn from consideration but not canceled: None.
3. Claims objected to: None.
4. Claims allowed or confirmed: None.
5. Claims rejected: 36-43.

#### C. CLAIMS ON APPEAL

The claims on appeal are: 40-43.

#### IV. STATUS OF AMENDMENTS

Appellants canceled claims 1-4, 11-15, and 21-25, and amended claims 32 and 40 in the amendment filed February 12, 2007. This amendment was denied entry by the Examiner on March 7, 2007. Appellants further canceled claims 1-4, 11-15, 21-25, and 32-39, and amended claim 40 on June 8, 2007. The Examiner entered this amendment on August 14, 2007.

Appellants agree with the Examiner that the Appellants' amendment on June 8, 2007 that amended claim 40 to add a semicolon had an incorrect status indicator. In particular, the status indicator stated "previously presented" when it should have read "currently amended." Appellants thank the Examiner for entering the amendment with the incorrect status indicator. Appellants are willing to submit a new amendment with the correct indicator if requested by the Examiner or the Appeal Board.

## V. SUMMARY OF CLAIMED SUBJECT MATTER

### 1. Introduction

The present application is directed toward solving the problem of data collisions on a bi-directional data bus in a memory system. In one embodiment shown in Figure 1, a memory system has multiple memory modules 130a-n connected to each other in series and to a memory hub controller 128 via a bi-directional data bus. Data collisions can occur on a bi-directional data bus when a read command is issued before a write command. For example, as read data is heading downstream from a memory device on memory module 130c and write data is simultaneously heading upstream from the memory hub controller 128 to memory module 130n, the read data and the write data would collide. The present application prevents this data collision by using a bypass circuit 286. In one embodiment, the bypass circuit 286 is capable of temporarily storing data passing through a respective memory hub 140. As in the example provided above, as the read data is about to head downstream toward memory module 130b from memory module 130c, the write data is heading upstream from memory module 130a toward memory module 130b. In order to prevent a data collision, the write data is temporarily stored in the bypass circuit 286 in the memory hub 140 of memory module 130b. While the write data is stored in the bypass circuit 286, the read data continues downstream to memory module 130a. Once the read data passes through memory module 130b on its way to memory module 130a, the write data may be recoupled to the bi-directional data bus to continue its way upstream to memory module 130n. Therefore, when a read command is issued before a write command, the corresponding write data can be sent upstream before the read latency of the previously issued read command is complete. *Specification*, at page 8, lines 12-27, page 10, lines 21-28, page 11, lines 1-22 and Figure 3.

### 2. Claim 40

Claim 40 is directed toward a method for executing read and write commands in a memory system having a bidirectional memory bus. *Specification*, at page 5, lines 15-17. The method of claim 40 includes "issuing a read command to access a first memory location in the memory system" and "before completion of the read command, scheduling a write command to

write data to a second memory location in the memory system." In one embodiment, a read command is issued by the memory hub controller 128 to access a first memory location in a memory system. Before completing the read command, a write command is scheduled by the memory hub controller 128 to write data to a second memory location in the memory system. *Id.* at page 10, lines 21-28.

In addition, claim 40 includes "retrieving read data from the first memory location." In one embodiment, the read data is retrieved from the first memory location. *Id.* at page 10, lines 21-28.

Claim 40 further includes "prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system." In one embodiment, prior to the memory hub controller 128 receiving the read data on the memory bus, the write data corresponding to the write command is provided to the bidirectional memory bus. *Id.* at page 10, lines 27-28 and page 11, line 1.

Claim 40 further includes "in the memory system, bypassing the read data on the bidirectional memory bus." In one embodiment, the read data on the bidirectional memory bus is bypassed while in the memory system when a bypass circuit 286 captures the write data so that read data can be sent to the memory hub controller 128. *Id.* at page 11, lines 1-14. Finally, claim 40 includes "receiving the read data on the bidirectional memory bus from the memory system" and "providing the write data to the bidirectional memory bus." In one embodiment, the read data on the bidirectional memory bus is received by the memory hub controller 128 from the memory system. *Id.* In addition, the write data is provided back to the bidirectional memory bus. *Id.*

## VI. GROUND OF REJECTION TO BE REVIEWED ON APPEAL

The only ground of rejection to be reviewed on appeal is whether claim 40, as well as any claims dependent thereon, are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent Application No. 2005/0105350 to Zimmerman (“Zimmerman”), in view of U.S. Patent No. 6,622,188 to Goodwin et al. (“Goodwin”) and further in view of U.S. Patent No. 6,901,494 to Zumkehr et al. (“Zumkehr ”). (Office Action dated December 5, 2006).

## VII. ARGUMENTS

I. Claim 40 are Patentable over Zimmerman in view of Goodwin and further in view of ZumkehrA. *The Subject Matter of Claims 40*

Claim 40 reads as follows:

40. A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system;

retrieving read data from the first memory location;

prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;

in the memory system, bypassing the read data on the bidirectional memory bus;

receiving the read data on the bidirectional memory bus from the memory system; and

providing the write data to the bidirectional memory bus.

B. *The Subject Matter Disclosed in the Zimmerman Reference*

The Zimmerman reference is directed to a memory test mechanism for buffered-memory-module memory subsystems. The Zimmerman reference provides a testing method for evaluating individual memory modules and individual module-to-module memory channels independent of the host and host memory channel. The Zimmerman reference is cited by the

Examiner for disclosing a memory system that includes multiple hub-based memory modules with data paths that interlink the memory module hubs. Although the Zimmerman reference does disclose the memory system described above, it and no other reference cited by the Examiner discloses data bypass capabilities when a read command is issued, and before the read latency is met, issuing a write command and corresponding write data.

***C. The Subject Matter Disclosed in the Goodwin Reference***

The Goodwin reference is directed to an I<sup>2</sup>C bus expansion apparatus that permits multiple bus devices of the same group to reside on an I<sup>2</sup>C bus in a data processing system. The I<sup>2</sup>C bus is a 2-wire bidirectional serial bus for communication between bus devices in a data processing system. The Goodwin reference is cited by the Examiner for disclosing a bidirectional data bus. Although the Goodwin reference discloses a bidirectional data bus, it and no other reference cited by the Examiner discloses data bypass capabilities when a read command is issued, and before the read latency is met, issuing a write command and corresponding write data.

***D. The Subject Matter Disclosed in the Zumkehr Reference***

The Zumkehr reference discloses a RAMBUS control and data bus connecting a RAMBUS memory controller 210 to a translator hub 220, and a SDRAM control and data bus connecting the translator hub 220 to SDRAM memory devices 161. *Zumkehr Specification*, Figure 2. SDRAM devices require write data to be sent with write commands. Therefore in prior systems, write commands were delayed until the write data could be sent from the RAMBUS memory controller to the SDRAM device via the translator hub. Therefore, both the write command and corresponding write data could not be sent until after the read latency of the previous read command was met. The Zumkehr reference, however, teaches the ability to issue a write command without sending the corresponding write data by storing the write command in a write buffer within the translator hub. By being able to send a write command without corresponding write data, the Zumkehr reference teaches the ability to issue a write command after a read command has been issued; however, the Zumkehr reference does not teach

the ability to issue the corresponding write data before the completion of the latency of the previous issued read command. *Zumkehr Specification*, column 4, lines 45-68 – column 5, lines 1-13.

In Figure 5A, the Zumkehr reference discloses a timing diagram of a memory system where the translator hub does not include a write buffer and Figure 5B shows a timing diagram where the translator hub does include a write buffer. In Figure 5A, a write command following a read command is delayed by a period corresponding to the read latency of the previous read command. In contrast, Figure 5B, which includes a write buffer in the translator hub, shows that a new write command 520B following a read command 501B can be issued before the read latency of the previously issued read command 501B is met. Once the new write command 520B is received in the translator hub, *a previous* write command 522B and corresponding write data 525B already stored in the translator hub are sent to the memory devices. However, the write data 527B associated with the new write command 520B remains in the memory controller and cannot be issued until *after* the read latency of the previously issued read command 501B is met. *Zumkehr Specification*, column 5, lines 39-44, column 6, lines 53-67 – column 7, lines 1-49 and Figures 5A and 5B. Therefore, the Zumkehr reference does not disclose or fairly suggest data bypass capabilities when a read command is issued, and before the read latency is met, issuing a write command and corresponding write.

#### ***E. Summary of the Rejection***

The final rejection dated December 5, 2006 rejects claim 40 as being unpatentable under 35 U.S.C. § 103(a) over Zimmerman, in view of Goodwin, and further in view of Zumkehr.

In the Office Action, the Examiner rejected claim 40 under the same rationale as cancelled claim 1. *Office Action*, page 5, line 7 and page 7, lines 8-13, respectively. Under claim 1, the Examiner contends that Zumkehr discloses a write bypass circuit coupled to a direct data path and temporarily storing write data to allow read data to be transferred through the direct data path while the write data is temporarily stored, the write bypass circuit further operable to recouple the stored write data to the direct data path after the read data is transferred

through the direct data path. In particular, the Examiner contends that the multiplexer or the write buffer in Figure 6 of the Zumkehr reference is analogous to the write bypass circuit of claim 1.

Claim 40 is patentably distinct from claim 1. Cancelled claim 1 disclosed a write bypass circuit coupled to a bidirectional data path capable of temporarily storing write data to allow read data to pass through the bidirectional data path and then recoupling the stored write data to the data path. Therefore, write data and read data could be on the bidirectional data path at the same time, moving in opposite directions and still avoid a data collision. Claim 1 did not require that the write command and corresponding write data be issued before completion of the read command. However, method claim 40 requires scheduling a write command to write data before completion of a previously issued read command.

It appears that the Examiner contends that the Zumkehr reference discloses a method of bypassing write data regardless of whether the latency of a previous read command is met. The Appellants contend that the Zumkehr reference does not disclose or fairly suggest the capability of preventing a data collision on a bidirectional data bus when a read command is issued followed by a write command and corresponding write data, when the write command and corresponding write data are issued before the read latency is met.

***F. The Zimmerman, Goodman, and Zumkehr References, in Combination or by Themselves, Do Not Disclose All of the Limitations of Claim 40***

The Zumkehr reference was cited by the Examiner for disclosing a method of bypassing the read data on the bidirectional memory bus of claim 40. The Examiner contends that the multiplexer 650 or the write buffers 330 within the translator hub 220 have the capability of storing write data in order to prevent data collisions on a bidirectional data bus similar to the bypass circuit of the present application. The Zumkehr reference, however, does not disclose or fairly suggest the capability of preventing a data collision on a bidirectional data bus when a read command is issued, and before the read latency is met, issuing a write command and corresponding write.

As described above, the Zumkehr reference discloses a bus connecting a RAMBUS memory controller 210 to a translator hub 220, and an SDRAM bus connecting the translator hub 220 to SDRAM memory devices 161. The write buffer in the translator hub is capable of receiving a write command at a different time than the corresponding write data and sending the write command and corresponding write data to the SDRAM devices. *Id.* at column 5, lines 39-44 and Figure 5B. This improves the performance of the data transfer, because the write command can be issued from the memory controller without requiring the corresponding write data to be sent from the memory controller one clock cycle later. For example, a situation in which the corresponding write data can not be sent with the write command exists when a read command has already been issued. The write data must wait for the read latency of the previously issued read command to be met before it can be transferred to the translator hub. *Id.* at column 7, lines 18-20 stating “the RAMBUS memory controller 210 defers write data transfer on a write command until the read latency of a previous read command is met”. Once the translator hub receives the new write command, *a previously issued* write command and corresponding write data that were stored in the translator hub *before* the read command was issued may be sent to the memory devices before the read latency of the read command is complete. See, *Id.* at column 6, lines 53-67 – column 7, lines 1-49, and Figure 5B. Therefore, only the write data that was already issued and located on the translator hub may go onto the data bus after a subsequent read command is issued. If write data were issued from the memory hub after a read command was issued, there would be a collision on the RAMBUS data bus as the read data is heading downstream to the memory controller and the write data is heading upstream to the translator hub. Therefore, the Zumkehr reference does not disclose or fairly suggest the capability of preventing a data collision on a bidirectional data bus when a read command is issued, but before the read latency is met, issuing a write command *and corresponding write data*.. Neither the Zimmerman reference nor the Goodman reference make up for the deficiencies of the Zumkehr reference.

Turning now to the claims, the Zimmerman, Goodman, and Zumkehr references, in combination or alone, do not disclose all the limitations of claim 40. A claim

rejected under 35 U.S.C. § 103(a) must teach or suggest all of the claim limitations. M.P.E.P. 706.02(j).

Method claim 40 requires, in part, issuing a read command, *before completion of the read command*, scheduling a write command, retrieving the read data, but prior to receiving the read data from the memory system, providing write data corresponding to the write command to the bidirectional memory bus, and in the memory system, bypassing the read data on the bidirectional memory bus. As alluded to above, the Zumkehr reference fails to disclose or suggest the above limitation. Rather, the Zumkehr reference waits for the read latency of a read command to end before issuing the write data that corresponds to a write command issued after the read command. In contrast, method claim 40 requires providing write data to the bidirectional memory bus prior to receiving the read data from the memory system. Therefore, claim 40 is allowable over the Zumkehr reference.

Neither the Zimmerman reference nor the Goodwin reference make up for the deficiencies in the Zumkehr reference discussed above. In fact, the Examiner explicitly admits in the Final Office Action dated December 5, 2006 that neither the Zimmerman reference nor the Goodwin reference disclose a bypass data path. *Office Action*, page 4, line 6.

For all of the reasons explained above, neither the Zumkehr reference, the Zimmerman reference, nor the Goodwin reference, in combination or by themselves, disclose or fairly suggest all elements of claim 40 in the present application. Therefore, the rejection of claim 40, as well as claims dependent thereon, should be reversed.

## VIII. CLAIMS APPENDIX

The text of the claims involved in the appeal are:

40. A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system;

retrieving read data from the first memory location;

prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;

in the memory system, bypassing the read data on the bidirectional memory bus;

receiving the read data on the bidirectional memory bus from the memory system; and

providing the write data to the bidirectional memory bus.

41. The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

## IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.

XI. CONCLUSION

For all of the reasons stated above, the rejection of claims 40-43 should be reversed.

Respectfully submitted,

DORSEY & WHITNEY LLP



Karen Lenaburg  
Registration No. 58,571

KL:sp

Enclosures:

Postcard  
Amended Appeal Brief Transmittal (+copy)

1420 Fifth Avenue, Suite 3400  
Seattle, WA 98101  
Tel: (206) 903-2399  
Fax: (206) 903-8820